DESIGN OF LOW POWER CARRY SKIP ADDER USING DTCMOS

T.R.Dinesh Kumar¹, K.Mohana Sundaram², M.Anto Bennet¹, Aruna.R³*, Meena.B³, M.Mohanapriya³

¹Faculty of Electronics and Communication Engineering, Vel Tech, Chennai, Tamilnadu, India
²Faculty of Electrical and Electronics Engineering, Vel Tech Multitech Dr. Rangarajan Dr. Sakunthala Engineering College, Chennai, Tamilnadu, India
³UG Student of Electronics and Communication Engineering, Vel Tech, Chennai, Tamilnadu, India

* Email: arunaraja95@gmail.com

Submitted: May 27, 2017   Accepted: June 15, 2017   Published: Sep 1, 2017

Abstract- In the domain of VLSI design, the adders are always meant to be the most fundamental requirements for processors of high performance and other multicore devices. It is found that power dissipation is a major problem in the electronic devices. Power management integrated circuit (PMIC) is emphasized as battery-powered portable electronics such as smart phone are commonly used. In this paper we are designing a carry skip adder which consumes less power than the other conventional adders using dynamic threshold complementary metal oxide semiconductor (DTCMOS). The circuit is designed using Tanner EDA simulator of 32nm technology. Also the circuit is compared with the CMOS technology methods.

Index terms: Carry skip adder, low power consumption, high performance, speed and delay parameters
The adders are most widely used digital circuits which performs addition of numbers. Especially processors and computers make use of adders in arithmetic logic units[1,2]. The other operations which they perform in the processors are calculating table indices, addresses, and increment and decrement operators. for eg., Ripple carry adder (RCA), carry look ahead adder (CLA), carry skip adder (CSKA), carry save adder (CSA) for multiple bit addition. The most basic circuits for adders are full adder, half adder and binary adder[3,4].

1.1 Analysis of adder circuits:

Full adder is a logic circuit which adds two input bits plus a carry-in bit and produces the outputs as a carry-out bit and a sum bit. Fig.1. The s0 of a full adder is obtained by XOR of two input bits A, B and the Cin bit. The following are the schematic and truth table.

![Full adder truth table & schematic](image1)

Fig.2. The two half adder circuits cascaded together forms a full adder circuit. Its schematic view is:

![Full adder circuit using gates](image2)
To add an N-bit number, multiple full adders are implemented in which they are cascaded in parallel. Hence we go for such multiple bit adders to reduce time consumption. RCA is a logic circuit in which each full adder’s carry out is given as the carry in for the next succeeding significant full adder. It is named so, as each carry bit gets rippled to the next stage. Now there exists a term propagation delay for such operation. It is the time elapsed between the application of the input and occurrence of its corresponding output[5,6].

Consider an example as NOT gate in which the output will be “1” when an input of “0” is given. The time taken for NOT gate’s output “0” after an input “1” is given to the NOT gate’s input is the propagation delay found here. Similarly we can say that the carry propagation delay is the time elapsed between the application of carry-in and the occurrence of the carry-out.

II. Existing Methodology:

A carry skip adder is a multiple bit adder which consists of a RCA with speed up carry chain known as skip chain. The chain is the distribution of ripple carry blocks constituting skip carry blocks finally gives a skip adder. The CSKA gives us a compromise between the RCA and CLA.

Fig.4. The 8-block CSA circuit and its corresponding implementation in cadence tool are shown below:
Features:
- It speeds up the computations during comparison with RCA reducing path delay.
- When both the inputs of CSKA are not equal, it skips that stage particularly since the carry propagator is a XOR operation that is always high in this condition.

Fig.5. Hence in CSKA, the linearity of carry chain delays with the size of inputs is progressed allowing carries to skip instead of rippling through them.

Fig.4 8-block CSA in cadence tool.

Fig.5 simulation of 8-block

Fig.8. The CSKA circuit using CMOS technology is designed as shown below:
Hence we could say that there was a reduction in power consumption and delay factors as shown in below table. Though the number of transistors used is increased but the delay has been reduced accordingly.

<table>
<thead>
<tr>
<th>FACTORS</th>
<th>RC A</th>
<th>2BLOC K CSKA</th>
<th>4BLOC K CSKA</th>
<th>8BLOC K CSKA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power(µW)</td>
<td>0.53</td>
<td>0.614</td>
<td>0.68</td>
<td>0.73</td>
</tr>
<tr>
<td>Delay(ns)</td>
<td>47.18</td>
<td>46.79</td>
<td>44.47</td>
<td>41.53</td>
</tr>
<tr>
<td>Transistors</td>
<td>160</td>
<td>186</td>
<td>214</td>
<td>258</td>
</tr>
</tbody>
</table>

III. Proposed Technique:

The DTCMOS technique is a concept in which the input voltage is greater than zero for NMOS and negative for PMOS. Hence accordingly the threshold voltage gets reduced. This
Design of low power carry skip adder using dtcmos technique uses the body terminal too along with the other three terminals as input signal. That is, the gate and the body terminal are shorted. Hence we can say,

\[ V_{bs} = V_{gs} \]  \hspace{1cm} (1)

![Figure 9 applied input signals](image)

Fig. 9. Also the relation of threshold voltage \( V_t \) and input signal is given by,

\[ V_{T0} = 2\phi_B + V_{FB} + 2q \varepsilon_s N_a (2\phi_B) \varepsilon_o x \]  \hspace{1cm} (2)

\( V_{FB} \) - flat band voltage
\( \phi_B \) - inversion layer voltage
\( N_a \) - channel doping,
\( \varepsilon_s \) - Si permittivity,
\( q \) - Electron charge.

**3.1. Dynamic thresholds are characterized as:**

The dynamic threshold characteristics of a circuit are specified by VIHD and VILD. Those are defined as:

VIHD - The minimum HIGH input level where the normal switching characteristics are observed during output transients.
VILD - The maximum LOW input level where the normal switching characteristics are observed during output transients.

![Figure 10 noise factor](image)
IV. Simulation Results:

The implementation of CSKA circuit was done successfully and their respective results were obtained in the motive to reduce the power consumption. Firstly, the full adder circuit is designed using which ripple carry adder are constructed. Later the complete CSKA circuit is obtained using tanner EDA simulator as shown in figure.11:

Fig.11: full adder design

Fig.12: ripple carry adder

Fig.13: carry skip adder
Design of low power carry skip adder using dtcmos

V. Conclusion:

Hence we can say that the circuit implemented using DTCMOS had much reduction of power consumption than the CMOS technology. Even the delay factor is reduced in this circuit as compared with the ripple carry adder.

REFERENCES


Design of low power carry skip adder using dcmos


