Implementation of 144 × 64 Pixel Array Bezel-Less Cmos Fingerprint Sensor

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Abstract

This paper proposes CMOS integrated 144 × 64 pixel array fingerprint sensor without a bezel electrode. In this paper, the architecture of CMOS capacitive fingerprint sensor readout circuit is presented for general type of a switched capacitive integrator scheme. The pipelined scan driver is included in the fingerprint sensor for fast image capture. It is implemented on 0.35 µm standard CMOS process technology. The operation is validated by SPECTRE for one-pixel and RTL simulation including logic synthesis for a full chip design on condition of 0.35 µm typical CMOS process and 3.3 V power. The layout is performed by full custom flow for sensor cell array and auto P&R for a full chip. The area of a full chip is 4943 µm × 3943 µm and the gate count is 542,000. The area of one-pixel is 48 × 48 µm². The pitch is 50 µm and image resolution is 508 dpi and power consumption is less than 3 mA.

Keywords
Bezel-less, capacitive fingerprint, fingerprint sensor, readout circuit, switched capacitive integrator.

The solid-state capacitive fingerprint sensors are adopted on mobile application environment like a mobile phone. As far as technology trends are concerned, CMOS semiconductor, ultrasonic, and optical methods have been applied to manufacturing processes of fingerprint recognition sensors. The capacitive fingerprint sensor by semiconductor standard CMOS process is the most excellent in the cost, authentication accuracy, and reliability. Most of them rely on capacitive coupling between the finger and matrix of small metal plates to detect ridges and valleys on the finger surface. Each plate forms a pixel of the resulting image and requires circuitry to measure the capacitance. One of the most important performances of a capacitive sensor is the sensitivity capability since the detected capacitance is very small of the order of femto-farads.

There are bezel and bezel-less sensors in the capacitive fingerprint sensors. However, fingerprint sensors applied to mobile phones recently are mostly bezel type in terms of technology and design. The image of the bezel fingerprint sensor is excellent because the terminals for directly injecting charges are in contact with the skin. At coating thickness over 200 µm thick, it is very difficult for capacitive fingerprint sensors to obtain fingerprint image because the greater the coating thickness between the sensor and the fingerprint, the lower the signal strength. As the molding thickness increases, the parasitic signal becomes rather bigger than the main signal, and various circuit techniques for solving the problem are proposed.

This paper proposes parasitic insensitive fingerprint sensor with the switched capacitor integrator (Jung et al., 2005; Liu et al., 2012; Jung, 2013; Yeo, 2013a, 2013b, 2014, 2015; Gao et al., 2014; Jung, 2014) and implements the area type 144 × 64 array fingerprint sensor LSI with pipelined architecture for high-speed image capture. The proper operation is validated by HSPICE for one pixel and RTL simulation including logic synthesis for a full chip design on condition of 0.35 µm typical CMOS process and 3.3 V power.
power. The layout is performed by full custom flow for one pixel and auto P&R for a full chip.

**Fingerprint detection circuit and chip architecture**

The pixel-level detection circuit of capacitive sensing has been introduced as shown in Figure 1 (Jung, 2016). The circuit can use the capacitive sensing range of full supply voltage, because it combines a passive and parasitic-insensitive integrator. The circuit is suitable for low voltage and low power applications. The sensor plate is shielded by a metal to prevent the noise from the circuit under the sensor plate, which forms a parasitic capacitance between the sensor plate and the metal shield. Cp1 must be removed, because it is very large compared to Cf. To remove this parasitic capacitance, the output is applied to the bottom node of Cp1 to maintain the same potential between the both nodes of Cp1, which maximizes the sensitivity of the fingerprint sensor.

Figures 2 and 3 show the functional block diagram and floor planning of 144 × 64 fingerprint sensor chip. General biometric sensors use analog-to-digital converter (ADC) and programmable gain amplifier (PGA) to get good image quality. The detected signal of a sensor pixel is amplified to get reasonable signal level.
Figure 2: Functional block diagram of fingerprint sensor chip.

Figure 3: Pipelined scan fingerprint sensor driver architecture.
for ADC, which might increase system complexity. This paper proposes a fingerprint sensor amplify the detected signal by integration times using variable clock generator shown in Figure 2 rather than an amplifier.

The 144 × 64 pixel array fingerprint sensor is implemented with 0.35 μm standard CMOS process. The proposed circuit is designed to adjust the charge integration time from 1 to 7 times of 16 clocks with a control of 3 bit signal ‘period’, so it takes up to 112 clock times per pixel. When integrating for 112 clocks at 10 MHz main clock, the designed fingerprint sensor chip takes about 922 ms to obtain a frame fingerprint image of 144 × 64 pixel array. Generally, the fingerprint sensor chip should take about 0.5 s or less to capture and authenticate the image. In this paper, the pipelined scan fingerprint sensor driver architecture was applied, which helps to reduce the fingerprint image capture time and power consumption effectively. Variable clock generator block generates ‘vclk_out’, ‘hold_out’, and ‘hold_nor’ signal. These signals are used to control pipelined scan fingerprint sensor driver architecture. The 144 × 64 sensor cell array with pipelined scan architecture was applied to the fingerprint sensor. The fingerprint sensor is consisted of 144 × 64 sensor cells array with YDEC and XMUX and 16 bits shift ring-counter. The 16 bits shift ring-counter generates a pipelined scan signal which controls parallel scanner to drive maximum eight sensor cells simultaneously. 2-stage of 16 by 18 XMUX selects a proper column output for the proper evaluation sensor cell. Two memory cells are used to capture fingerprint output image. Figure 5 shows RTL simulation result of the proposed pipelined architecture. The fingerprint sensor proposed in the pipeline structure takes about 150 ms to capture the image, resulting in excellent response speed and low power consumption.
VLSI implementation

Figure 6 shows 144 × 64 pixel array chip layout and the die size is 7,569 μm × 4,569 μm on 0.35 μm standard CMOS process. The circuit includes two compiled SRAM memories, IO slot and analog block with ADC, PGA. The layout area of one pixel is 48 μm × 48 μm and pixel pitch is 50 μm. The gate count is 653,491. The layout of 144 × 64 array core cell is performed by full custom design method and the full chip is performed by auto placement and routing of cell-based design method.

Conclusions

This paper implements 80 × 64 array high sensitive fingerprint sensor with the parasitic insensitive charge transfer integrator. The fingerprint sensor core uses an active output voltage feedback integrator. The detection circuit of one pixel includes a pixel level charge transfer and parasitic insensitive integrator with a differential amplifier with pmos input. A multiple integration scheme is proposed to improve signal-to-noise ratio and amplify the sensing signal, which enables and robust fingerprint sensor driver architecture. The parasitic insensitive charge transfer circuit includes a simple differential amplifier and two switches to remove parasitic capacitance and transfer charge. The operation is validated by HSPICE for one pixel and RTL simulation including logic synthesis for the full chip design on condition of 0.18 μm typical CMOS process and 1.8 V power. The voltage difference between a ridge and valley is about 215 mV after 10 clock cycles and 367 mV after 20 clock cycles. The maximum frequency of cell operation is 10 MHz. The simulation results show the parasitic insensitive characteristics which increase touch sensitivity of the circuit. Full chip logic is synthesized and integrated with 80 × 64 array sensor core. The layout is performed by full custom flow for one-pixel and auto P&R for the full chip. The area of the full chip is 19.5 mm² (4,943 μm × 3,943 μm) and the gate count is 542,000. The area of one-pixel is 50 μm × 50 μm. Pitch is 50 μm and image resolution is 508 dpi.

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Literature Cited


