A promising optoelectronic clock solution for time-interleaved ADC

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Abstract—**A promising optoelectronic clock solution with low jitter, high bandwidth and accurate delay for a TIADC is proposed by exploiting optical pulses and tunable optical delay lines. It is feasible to construct the optoelectronic clock system with optical pulse source, dispersive medium, tunable delay line in optical domain and conditioning circuits in electronic domain while photodiodes as the bridge. The testing result of the designed conditioning circuit shows that using electronic method to adjust the signal will induce jitter degradation of the optoelectronic clock system.**

Keywords-analog to digital conversion; time-interleave; sampling jitter

I. INTRODUCTION

Analog-to-digital converter is an important element in measurement system, which converts the continuous signal to binary sequences suitable for digital processing. ADCs with high bandwidth and high resolution are need in special measurement areas such as radar and satellite communication. It is difficult for a single electronic ADC chip to capture an ultrafast signal with high precision. Therefore, we usually use a set of conventional electronic ADC chips in a parallel structure to alternately sample the ultrafast signal, which is called time-interleaved ADC (TIADC) system [1], as shown in Fig.1.

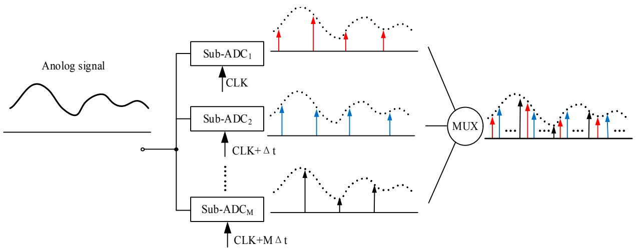

Figure 1. Structure of time-interleaved ADC system with M channels

In a TIADC system, there are M parallel electronic ADC chips. Each sub-ADC has a low sampling rate, f_s, and a high resolution, N bits. The sub-ADCs sample the input signal alternately with a fixed interval, $(1/f_s)/M$. In the digital domain, all quantization values merge into one sequence. Thus, the overall sampling rate is M times higher than an individual ADC while the effective number of bits of the system keeps N bits. In the TIADC system, the frequency of each sampling clock should be the same as the sampling rate of the sub-ADC, f_s and the time delay between adjacent channels should be $(1/f_s)/M$, as shown in Fig. 2.

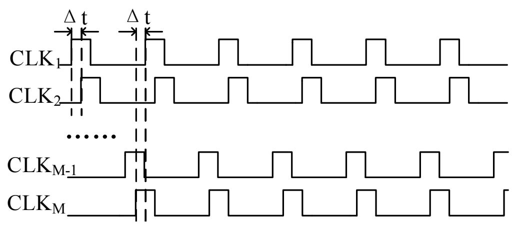

Figure 2. Staggered sample clocks for a time-interleaved ADC with M channels

The jitter of the sampling clock and the error of delay time affect the bandwidth and the resolution of the TIADC system, especially when the bandwidth of the input signal increases to radio or microwave frequency [2].

Jitter around the ideal sampling time edge may trigger an ADC to capture the signal at a wrong time, producing an error in the digitization output. The relation between the effective number of bits and the clock jitter [3] can be expressed as

$$ENOB = \log_2\left(\frac{1}{\sqrt{3}\pi f_{\text{sample}}\sigma_{\text{jitter}}}\right) \quad (1)$$

where $ENOB$ is the effective number of bits, f_{sample} is the sampling frequency and σ_{jitter} is the root mean square (RMS) value of the timing jitter.

According to (1), we find that to acquire a 2GHz signal with 8 bits effective numbers, the bandwidth of the ADC system should be higher than 4GHz while the maximum jitter of the sampling clock should be less than 0.1fs. As the frequency of the input signal increases, the requirements for high bandwidth and low clock jitter of the ADC system would be more severe. Unfortunately, due to the limitation of integrated circuit design and electromagnetic interference (EMI), recent electronic clock system can only offer a sampling clock with a few Giga-Hertz bandwidth and hundreds of femtoseconds jitter [4]. In contrast, optical pulses have the properties of ultralow timing jitter (on the order of attosecond) [5] [6], high repetition rate (160GHz) [7], high stability and strong immunity, which show tremendous potential to be the clock reference for ADC systems.

As for the delay errors, they are systemic errors and may lead to signal distortion. Because of the delay errors, the sample intervals of a TIADC system are heterogeneous. Consequently, when the quantization values are mixed into one sequence,

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signal distortion will occur. In traditional electronic clock systems, the electrical devices need tens of picoseconds to response and the length of the propagation paths of the clock pulse trains are not perfectly consistent with the theory values, so it is difficult to obtain a high speed multichannel clock with accurate time delay. Compared to the electrical implementation, optical time delay techniques have a number of advantages. The optical delay is inherently stable, wideband and immune to the electromagnetic interference and can be tuned accurately [8][9][10]. For example, the tunable precision of single mode fiber is 5ps and that of optical MEMS technology is 0.2ps [11].

In this paper, a promising optoelectronic multichannel clock solution with the properties of low jitter and accurate delay for a TI-ADC system is proposed. The proposed clock solution exploits optical pulse streams and optical delay lines in generating the multichannel clock. The implementation and feasibility analysis of the proposed clock solution are demonstrated as followings. Moreover, the design and test results of the conditioning circuit are provided.

II. OPTOELECTRONIC CLOCK SYSTEM

A. Implementation of the Optoelectronic Clock System

The layout of a four-channel optoelectronic clock solution is presented in Fig.3. It consists of an optical pulse source (the mode lock laser), an optocoupler, dispersive medium (the dispersion compensation fiber), tunable delay lines (the single mode fiber), photodiodes and conditioning circuits.

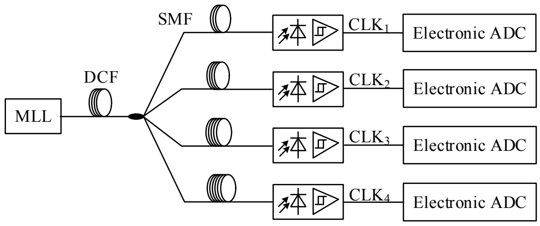

Figure 3. Architecture of the optoelectronic clock system for TIADC. MLL: mode locked laser. DCF: dispersion compensation fiber. SMF: single mode fiber.

The mode locked laser (MLL) with extremely low frequency noise generates an ultra-low-jitter optical pulse train with repetition period *T*. After propagating through the DCF, the duration of the optical pulse is stretched to tens of picoseconds in time domain, which offers sufficient time for the optical-electronic devices to respond correctly. Then the pulse stream is split into four channels with an optical coupler. The streams are passed through a set of delay lines which introduce incremental time delays of *T*/4 between them. Each of these optical pulse trains is detected by a photodiode. Before fed into the sub electronic ADCs, the electronic pulse trains should be modulated to differential pulse pairs within proper voltage range.

B. Feasibility of the Optoelectronic Clock System

The width, repetition rate and timing jitter of the optical pulses are dependent on the architecture of the mode locked laser [12]. Actively MLL can generate pulse streams with a high temporal stability and very low timing jitter, but the repetition frequency is limited by the relatively low frequency of the electronic modulation of the pump current. In contrast, passively mode locked laser can achieve a higher repetition frequency up to 160GHz with a relatively bigger timing jitter. In fact, it is available for a commercial MLL with the properties of high pulse repetition rate (up to tens of GHz) and low timing jitter (few femtoseconds).

When the pulse propagates through the dispersion compensation fiber (DCF), different frequency components take different time, so the pulse broadens itself in time domain. This stretching process is independent of the initial time of the pulse, so it has no influence on the timing jitter. The time scale of the stretched pulse is related to the length of the DCF as

$$\Delta t = D \cdot \Delta\lambda \cdot L \qquad (2)$$

where *D* is the dispersion parameter, $\Delta\lambda$ is the wavelength bandwidth of the pulse and L is the length of the DCF. For example, to stretch the duration of a transform-limited Gauss pulse from 200fs to 50ps, the required length of DCF with dispersion parameter -130ps/km/nm is only 22m.

It is easy to split the pulse train into 4 channels with a directional fiber coupler which introduces 6dB insertion loss.

When the pulse passes through a single mode fiber, the time delay can be calculated as

$$\tau = \frac{L \cdot n_{\text{eff}}}{c} \qquad (3)$$

where *L* is the length of the fiber, n_{eff} is the effective refraction index and *c* is the light velocity in the vacuum. Assuming the repetition period of the optical pulse is 1ns, the time delay between two adjacent pulse trains should be 250ps which equals to 1ns/4. According to (3), the length difference of the SMF between adjacent channels is 5cm, which is easy to achieve with an error on the order of picosecond.

After the optical pulses are stretched and delayed, photodiodes with tens of picoseconds of rise time are needed to convert them to electronic pulses. Since the stretching process reduces the peak power of optical pulses, it is achievable for the photodiodes to work at their linear regime and place little influence on the timing jitter and delay error. In addition, it is necessary for photodiodes to respond well in the spectral region of the optical pulses.

The weak electronic pulses from photodiodes can't be fed into the electronic ADCs directly, because high speed ADC chips usually need differential clocks with a peak to peak voltage on the order of hundreds of millivolts. Therefore, electronic conditioning circuits are needed.

III. EXPERIMENT AND DISCUSSION

In the experimental setup, as Fig.4 shows, a distributed feedback laser (Santec TSL-510), a Mach-Zehnder intensity modulator and an electronic signal source (Tektronix AFG3252) are used to generate the optical pulses. The center wavelength of the continuous light from the DFB laser is 1550nm. It is intensity modulated in the MZM by a 100M sinusoidal wave from the radio signal source. Then a sinusoidal optical clock signal is obtained from the output of the MZM. Compared to using an MLL to generate optical pulses, the advantage of this method is

low-cost and adjustable and the main drawback is that the clock jitter is limited by the electronic radio source. At the preliminary stage of the optoelectronic study, we choose this adjustable method as optical clock source.

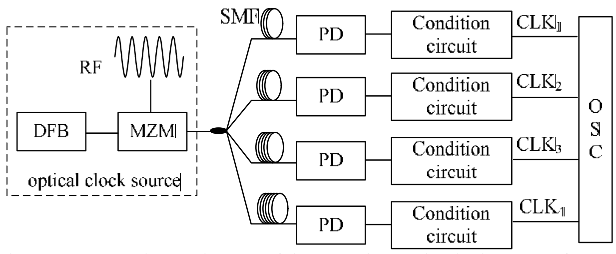

Figure 4. Experimental setup of the optoelectronic clock system for a two channel TIADC. DFB: distributed feedback optical source. MZM: Mach-Zehnder intensity modulator. SMF: single mode fiber. PD: photodiode. OSC: oscilloscope.

In the experimental setup, as Fig.4 shows, a distributed feedback laser (Santec TSL-510), a Mach-Zehnder intensity modulator and an electronic signal source (Tektronix AFG3252) are used to generate the optical pulses. The center wavelength of the continuous light from the DFB laser is 1550nm. It is intensity modulated in the MZM by a 100M sinusoidal wave from the radio signal source. Then a sinusoidal optical clock signal is obtained from the output of the MZM. Compared to using an MLL to generate optical pulses, the advantage of this method is low-cost and adjustable and the main drawback is that the clock jitter is limited by the electronic radio source. At the preliminary stage of the optoelectronic study, we choose this adjustable method as optical clock source.

The optical clock is split into four channels by a fiber coupler. The fiber coupler is single mode at the wavelength of 1550nm with a maximum insertion loss 6.43dB. The polarization dependent loss of the fiber coupler is less than 0.15dB, which has little influence on the sinusoidal optical clock signal. In this experiment, only one channel is setup completely.

Photodiode module with 10GHz bandwidth and 35ps rise time is used to convert the optical waves to electronic waves.

The electronic waves from photodiodes has high frequency, 100MHz and low peak to peak voltage level, 8mV. A special conditioning circuit is designed to amplify and adjust the signal. The block diagram of the conditioning circuit is shown in Fig.5.

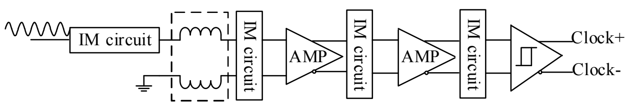

Figure 5. Block diagram of the conditioning circuit. IM circuit: impedance matching circuit. AMP: amplifier.

Coaxial cable is used as the transform medium which offers a good immunity to the electromagnetic interference of the environment. To get good interface with the photodiode, low load resistance and capacitance are offered to ensure the detector with an ultra-low rise time. The single-ended clock wave is converted to differential signal by a wideband transmission line transformer with a 1:1 impedance ratio. Then the differential clock signal is magnified by two cascaded differential amplifiers to be suitable for the comparator. The comparator can suppress the noise near zero voltage due to the hysteresis effect and offer RSPECL (reduced swing positive emitter-coupled logic) output to drive the electronic ADC chip. Impedance matching circuits are designed according to the datasheets of the electronic devices. During the PCB layout, the differential clock traces are well matched.

The output signal (at 200MHz) of the clock system is detected by Agilent oscilloscope (MSO9254A), as shown in Fig.6. The eye diagram presents lots of waves in one screen. The RMS jitter of the optoelectronic clock signal is about 11ps calculated by the oscilloscope.

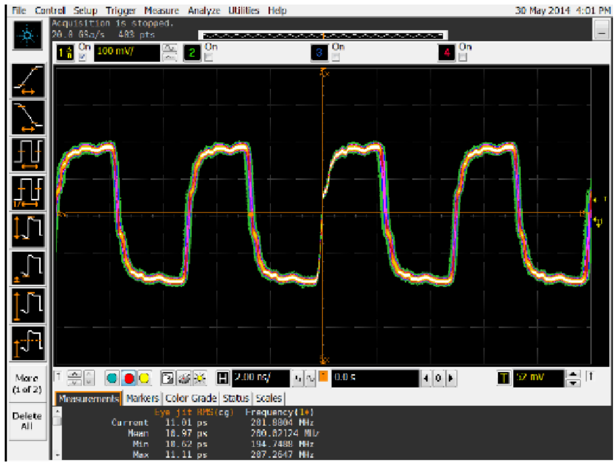

Figure 6. Eye diagram of the optoelectronic clock signal

To confirm the main part inducing the timing jitter, another experiment is operated. The electronic signal is directly feed into the conditioning circuit and the output signal is also detected by MSO9254A. Fig.7 shows the result. The RMS jitter induced by the electronic module is about 10ps.

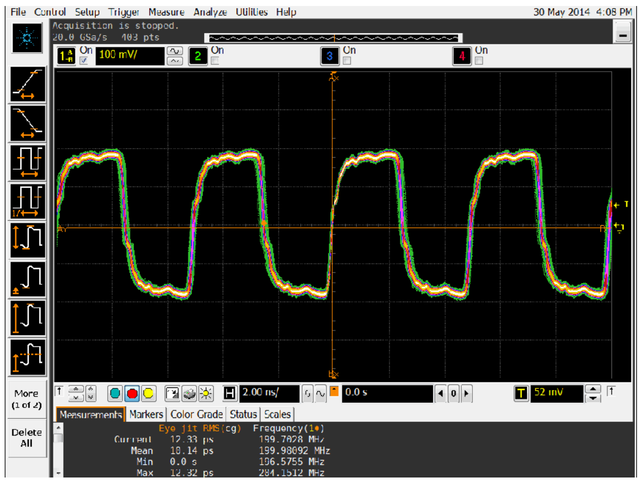

Figure 7. Eye diagram of the electronic module signal

The jitter is mainly caused by the conditioning circuit, because the electronic amplifiers and comparator need long response time and the threshold voltage of the comparator is fluctuant which leads to variable propagation delay. In addition, the electronic signal source and the oscilloscope also influence the timing jitter. This result indicates that to get good extension of the low jitter of the optical clock, electronic devices should be used as few as possible.

IV. CONSLUSION

An optoelectronic multichannel clock solution for TIADC system is demonstrated in this paper. This solution utilizes optical pulses as the clock reference and employ optical delay technique to get accurate delay. Compared to all-electronic clock system, the proposed optoelectronic clock can provides low clock jitter and high precise delay. The jitter of the optoelectronic clock system constructed with DFB and MZM instead of MLL and DCF is 11ps, mainly caused by the electronic devices in the conditioning circuit. This result indicates that it is necessary to improve the conditioning circuit or exploit other methods to modulate the optoelectronic clock signal.

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