Dual Slope Direct Digital Converter for Bridge Connected Resistive Sensors

Ponnalagu R. N, Boby George, Member IEEE, and Jagadeesh Kumar V, Senior Member IEEE
Department of Electrical Engineering, Indian Institute of Technology Madras, Chennai 600036, India.

Abstract—A dual slope direct digital converter (DSDDC) suitable for resistive sensor elements already connected in a bridge form is presented. A conventional dual slope analog to digital converter (DS-ADC) is altered with an intentionally introduced instrumentation amplifier (INA) to realize the proposed DDC. The DSDDC accepts bridge connected resistive sensor elements as input and provides a digital output that is proportional to the quantity being sensed by the sensor elements. The results obtained from simulation of the proposed DSDDC indicate a worst case error in the output to be <±0.03 %. Experimental results from a prototype unit, presented herein, demonstrate the practicality the scheme. Worst case error of the prototype unit was found to be <±0.07 % with test conducted using standard decade resistance boxes emulating the sensor elements. The worst case error in the prototype was <±0.05 % when tested with a load-cell made of four strain gauges.

Keywords- Direct digital converter; Resistive sensors; Strain gauges; Wheatstone bridge; Instrumentation amplifier; Dual slope digital converter;

I. INTRODUCTION
Resistive sensing elements are popular for sensing several physical parameters such as displacement (linear and angular), strain, force, pressure, temperature and torque [1] - [5]. The performance of such resistive sensor elements is affected by environmental factors. For example, variation in the operating temperature of a resistive strain gage introduces an error in its strain sensing characteristics [6]. It is possible to eliminate the temperature effect with either two (half-bridge) or four active sensor elements (full-bridge) connected to form a Wheatstone bridge circuit [4] - [6]. Use of two or four active resistive sensor elements in a bridge form, apart from providing temperature compensation, provides increased sensitivity and linearity at the output. Sensors are interfaced to a digital instrumentation system to exploit the processing power and better user interface available with digital instrumentation systems. To interface resistive type sensor(s) to a digital instrumentation system, first an analog signal conditioning circuit is employed to convert the variation in the resistance(s) of the sensor element(s) into an analog voltage. The analog voltage is then converted to digital utilizing an analog to digital converter (ADC). It would be advantageous if we can interface the resistive elements directly to a suitable ‘resistance to digital converter’, dispensing with the analog signal conditioning circuit [7]. Such a direct digital converter (DDC) will possess advantages such as reduced complexity, reduced power and increased reliability. Due to this fact, schemes that convert the variation in the resistances of sensor elements into quasi-digital forms like frequency and time period have been proposed [8], [9]. However, such schemes require additional interface to convert the quasi-digital outputs into digital. It is reported that such methods suffer due to change in temperature and aging [10] – [12]. Direct Digital Converters (DCC), where the sensor elements are directly operated by an analog-to-digital converter, eliminating the intermediate analog signal conditioning circuit, have been proposed [7], [13] - [15]. The DDC reported earlier for two or four resistive sensors in bridge form requires three integration periods for conversion [15].

We now present a dual slope type direct digital converter that accepts resistive sensor elements in a bridge circuit form and provides a digital output proportional to the physical quantity being sensed by the resistive sensor elements. Compared to the scheme reported earlier [15] that requires three integrations for a conversion, the present scheme requires only two integration periods and hence will be 33 % faster than the previous scheme. The proposed scheme easily handles resistive sensor elements with low sensitivity.

II. PROPOSED DUAL SLOPE DIRECT DIGITAL CONVERTER
The block schematic of the proposed dual slope direct digital converter is shown in Fig. 1. The sensor elements $R_1, R_2, R_3$ and $R_4$, are connected in a Wheatstone bridge form. As in any bridge form of sensor elements, here too, the elements are arranged such that resistances of elements $R_2$ and $R_3$ increase with the physical quantity, say $x$, being sensed. On the other hand, resistances of elements $R_1$ and $R_4$ decrease with increasing $x$. In such a case the resistances of these sensing elements can be expressed as:

$$R_1 = R_4 = R_0 (1 \pm kx) \quad (1)$$
$$R_2 = R_3 = R_0 (1 \mp kx) \quad (2)$$

In (1) and (2), $k$ represents the transformation constant of the sensor elements and $R_0$ indicates the nominal value of the sensor element when $x$, the physical quantity being sensed by it, is zero.

As in a conventional dual slope ADC, the proposed DSDDC also contains a control and logic unit (CLU) with an integral timer-counter, an integrator (opamp $O_{I_2}$ with capacitor $C_I$ in its feedback and input resistor $R_I$), and a comparator as indicated in Fig. 1. The output voltage of integrator, $v_{I_2}$, is fed as input to comparator $OC$ which is configured as a zero crossing detector. The comparator output will be high if $v_{I_2}$ is positive and it will be low if $v_{I_2}$ is negative. A high to low or low to high transition indicates zero crossing. It is easily seen in Fig. 1 that node $p$ of the sensor bridge is connected to the
output of opamp OA1, which provides the necessary excitation to the bridge. The node \( q \) of the bridge is connected to ground
and the nodes \( s \) and \( r \) are connected to the inputs of opamps
OA1 and OA2. Opamps OA1, OA2 and OA3 constitute a modified
instrumentation amplifier, INA. The SPDT switch \( S_2 \)
configures opamp of OA1 to be a differential (\( S_2 \) in position 0)
 or summing amplifier (\( S_2 \) at position 1).

The CLU senses the output of comparator \( v_c \), generates
necessary switching signals and achieves required sequence of
operations required to implement the logic of the proposed
DSDDC. A typical conversion cycle of the DSDDC is made of
two distinct phases of operation, namely, an auto-zero phase
and a conversion phase. An auto-zero phase precedes a typical
conversion phase so as to ensure that the output of the
integrator is made zero, a condition essential for proper
operation of the dual slope principle. For continuous
conversion (a new conversion succeeding a previous one,
endlessly), the auto-zero phase is needed only once at the start,
since at the end of a conversion, the integrator’s output will be
zero and hence a new conversion can start without an auto-zero
phase.

A. Auto zero phase

In the auto-zero phase, the CLU senses \( v_c \). If \( v_c \) is high (\( v_c \) is
positive) the CLU sets the switches \( S_1 \) and \( S_2 \) to position ‘1’.
In this situation \( OA_3 \) will act as an inverting amplifier
providing a voltage of \(-V_R\) to node \( p \) and \( OA_3 \) will act as an
inverting summing amplifier and its output \( V_o \) will be
\(-V_1 - V_2\), where

\[
V_1 = \frac{V_p (1 \pm kx)}{2} \quad \text{and} \quad V_2 = \frac{V_p (1 \mp kx)}{2}.
\]

\( V_p \) is the voltage at node \( p \). \( V_p = V_R \) when \( S_1 \) is in position ‘0’
and \( V_p = -V_R \) when \( S_1 \) is shifted to position ‘1’. For the
condition \( S_1 \) and \( S_2 \) in position ‘1’, a current \( i_c = -V_R/R_7 \) will
flow and discharge the capacitor \( C_1 \). Thus, the integrator output
will start decreasing and reach zero as shown in Fig. 2 by the
dashed line shown during the auto-zero phase.

On the other hand if \( v_c \) is low (indicating a negative \( v_{oi} \)) the
CLU will set switch \( S_1 \) to position ‘0’ and \( S_2 \) to position ‘1’. In
this case \( OA_3 \) will act as a buffer giving \(+V_R\) to node \( p \) and \( OA_3 \)
will again act as a summing amplifier and its output will be
sum of \( V_1 \) and \( V_2 \). Now current \( i_c = V_R/R_7 \) will flow. Once
again the charge in the capacitor \( C_1 \) will be removed resulting
in the integrator output rising to zero from the negative initial
condition.

In either case, when the integrator output reaches zero,
output of the comparator will flip (‘1’ to ‘0’ in the first case
and ‘0’ to ‘1’ in the second case) signaling the end of auto-zero
phase to the CLU. The CLU sensing the flip in \( v_c \) starts a
conversion phase.

B. Conversion phase

The conversion phase, as in any dual slope converter, has a
pre-set integration period \( T_1 \) and a measured de-integration
period \( T_o \). At the start of a conversion phase, the CLU sets
switches \( S_1 \) and \( S_2 \) in position ‘0’ and initiates the first
integration period \( T_1 \). The CLU starts the internal timer

![Fig. 1. Block schematic of the proposed DDC for bridge connected resistive sensors](image-url)

![Fig. 2. Waveforms at cardinal points of the proposed DDC](image-url)
simultaneously and maintains the switch positions for the first integration period for a certain count, say \( N_i \) \( (T_1 = N_i \ T_c) \), where \( T_c \) is the period of the clock fed to the timer-counter of the CLU). For this case, the output \( V_o \) of opamp \( OA_3 \) is:

\[
V_o = -G(V_i - V_x) \tag{5}
\]

where \( G = [1 + 2(R/R_o)] \). If the physical quantity being sensed, \( x \), is positive then \( R_2 > R_1 \) and hence the current \( i_c = V_o/R \) will flow into the capacitor \( C_1 \) of the integrator and the integrator output \( V_o \) will ramp up (indicated as solid line in Fig. 2) with time as:

\[
v_o = \frac{G(V_i - V_x)}{R_c} t = V_o G k x t \tag{6}
\]

At the end of \( T_1 \), the CLU is programmed to sense the comparator output \( v_c \). Since \( v_c = '1' \) (for positive \( x \)) the CLU logic changes the position of switches \( S_1 \) and \( S_2 \) to position '1' and restarts the timer counter. For this condition the output \( V_o \) of opamp \( OA_1 \) will be

\[
V_o = -G(V_i + V_x) = V_o 
\]

The current through \( C_1 \) will now be \( i_c = -V_o/R \). This current will discharge the capacitor \( C_1 \) forcing the output voltage of the integrator to decrease with time and reach zero. As soon as the output of the integrator reaches zero, the output of the comparator will change state signaling to the CLU that the conversion phase is over. The count value at this point, say \( N_o \), from the timer-counter is read by the CLU and displayed as the final output.

If \( x \) is negative \( (R_2 < R_1) \) then during the first integration period \( T_1 \), the integrator output will increase in the negative direction and at the end of \( T_1 \) will be \( -V_o G k x T_1 \). Hence at the end of \( T_1 \), the output \( v_c \) of the comparator will be '0'. Sensing \( v_c \) to be '0' the CLU sets switch \( S_1 \) in position '0' and \( S_2 \) in position '1' and restarts the timer-counter. The voltage on node \( p \) will now be \( +V_o \) and \( V_o = -(V_i + V_x) = V_o \). Thus a current \( i_c = V_o/R \) will flow into \( C_1 \), discharging it. For this case, the integrator output will ramp up and reach zero as indicated by the dashed line (during conversion phase) in Fig. 2. Once again the comparator output will flip (from '0' to '1') as soon as the integrator output reaches zero. Sensing the flip, the CLU stops the timer-counter, reads the value of the timer-counter and displays it as the output.

In either case \( (x \) is positive or negative), the charge acquired by the capacitor \( C_1 \) during \( T_1 \) must be equal to the charge removed from \( C_1 \) during \( T_2 \) since the net charge in \( C_1 \) at the end of \( T_o \) is zero. The charge balance results in:

\[
\frac{G(V_i - V_x)}{R_c} T_1 = \frac{(V_i + V_x)}{R_c} T_o \tag{7}
\]

Substituting the values \( V_1 \) and \( V_2 \) from (3) and (4) into (7) we get:

\[
G V o T_1 = V o T_o \tag{8}
\]

By rearranging (8), \( x \) is derived as:

\[
x = \frac{1}{k G T_1} T_o \tag{9}
\]

Since \( T_1 = N_i T_c \) and \( T_o = N_o T_c \), (9) can be simplified as:

\[
\text{The polarity of } x \text{ can be easily determined by sensing the output } v_c \text{ of comparator at the end of period } T_1. \text{ The sequence of operations of the DSDDDC is clearly depicted in the flowchart shown in Fig. 3.}

\[
\text{III. SIMULATION STUDIES}
\]

The functionality of the DSDDDC presented here was first checked by simulating the circuit using circuit simulation tool, LTSpice. The opamps used in the simulation are selected to match the performance and characteristics of practical opamps, later used to build the prototype DSDDDC. The control logic is simulated by using four switches controlled by pulse waveforms and logic gates. The nominal values \( (R_o) \) of four resistors were set as 1.0 kΩ and resistances were varied in steps of 10 Ω in the range 900 Ω to 1100 Ω \( (kx = \pm 10\% \text{ of } R_o) \). The output obtained from simulation was plotted and a best fit also obtained for that which is clearly indicated in Fig. 4. The worst case error obtained after employing best fit using linear regression analysis is found to be \( < \pm 0.03\% \).

\[
\text{IV. EXPERIMENTAL RESULTS}
\]

In order to verify the practicality of the proposed DSDDDC, a prototype unit was built and tested. The reference voltage \( V_o \) was obtained using reference voltage generator IC LM385. All the opamps in the circuit of Fig. 1 are of type: IC OP07. The
switches $S_1$ and $S_2$ were realized using IC MAX 4602, possessing quad SPST switches having ON resistance of 2.5 $\Omega$. To obtain the SPDT operation required for switches $S_1$ and $S_2$, each SPDT switch was realized by connecting two SPST switches in parallel. While the control of one of the parallel connected SPST switch was fed directly from the CLU, the control of the other switch was fed through a NOT gate (IC SN7404). The feedback capacitor of the integrator was selected to be polypropylene type of value 0.33 $\mu$F and a metal film resistor of value 100 k$\Omega$ served as $R_i$. IC LM311 was used as the comparator.

The Control and Logic Unit was implemented with an Arduino UNO board containing an ATMEGA 328 microcontroller [16]. The Arduino board was interfaced to a personal computer (PC) utilizing the onboard USB interface. The PC not only served to cross compile and program the microcontroller, but also served as the output display. A suitable program, developed to implement the necessary logic illustrated in the flowchart of Fig. 3, is burnt into the microcontroller [17]. The program makes use of one of the timer-counters of the microcontroller for realizing the timing/counting operations outlined in Fig. 3. Using the internal clock of the microcontroller, the first integration period $T_i$ is set as 300 ms. The output $N_1$ is obtained in terms of counts read from the internal counter-timer and the count values are displayed on the PC.

In order to obtain the performance characteristics of the proposed DSDDC under controlled input conditions, sensor elements $R_1$, $R_2$, $R_3$ and $R_4$, were realized using standard variable resistance boxes form Otto Wolff, Germany having a resolution of 1.0 $\Omega$ and an accuracy of $\pm$0.01%. $R_a$ for all the four resistors was selected to be 1.0 k$\Omega$ and the measurements were obtained by varying the physical quantity $x$ in steps of 0.01 from -0.1 to +0.1 through zero. The results obtained from this emulation test of the prototype are shown in Fig. 5. The worst-case error observed from the emulation study was found to be $< \pm$0.07%.

To establish the suitability of the proposed DSDDC for a practical application, the prototype unit was also tested using a load cell made of four resistive strain gauges connected in bridge form. The experimental setup utilized for conducting this test is shown in Fig. 6. The load-cell used is a standard aluminum single point, 290 $\Omega$ nominal value load cell of full scale 3.0 kg and sensitivity of 0.48 m$\Omega$/kg. The feedback capacitance, $C_i$ was chosen as 100 nF. The load cell was loaded in the 0 kg to 3 kg range in steps of 250 g. While it was possible to vary $kx$ both in the positive and negative directions in the emulation study, $kx$ varied only in the positive direction in the tests carried out with the load cell. The snapshot of integrator output, $v_{oi}$ and comparator output, $v_c$ for a typical $kx$ value obtained from the prototype using the oscilloscope module of NI ELVIS II is shown in Fig. 7. The results obtained with the load cell, plotted in Fig. 8, illustrate that the worst case error is $< \pm$0.05%.

![Fig. 4. Results of simulation studies](image1)

![Fig. 5. Experimental results obtained by emulating the sensor resistors $R_1$, $R_2$, $R_3$ and $R_4$ using standard resistance boxes](image2)

![Fig. 6. Experimental setup to test the proposed DDC](image3)

![Fig. 7. Snapshot of integrator and comparator output waveforms observed from the prototype.](image4)
V. CONCLUSION

A dual slope type direct digital converter (DSDDC) that provides a digital output linearly proportional to the input quantity being sensed by bridge connected resistive sensing elements is presented. The Wheatstone bridge configuration of sensing elements becomes an integral part of a suitably augmented dual slope analog to digital converter. The dual slope digital converter in conjunction with a modified instrumentation amplifier enables conversion of the physical quantity being sensed by the resistive elements directly into digital form.

The suitability of the proposed scheme even for resistive sensing elements possessing very low sensitivity ($10^3$) has been established with tests conducted on a load cell made of strain gauges possessing a gage factor of 2.5. Since the proposed DSDDC is of dual slope type, all the advantages of the dual slope principle such as good resolution, accuracy, tolerance to component variations and immunity from noise and interference are applicable to the proposed DSDDC. Results obtained from (i) simulation study, (ii) emulation study and (iii) practical experimentation using a strain gauge type load cell on a prototype DSDDC establish the efficacy of the proffered scheme.

REFERENCES