A Capacitance-to-Digital Converter with Sinusoidal Excitation Suitable for Series RC Sensors

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Abstract—A new Capacitance-to-Digital Converter (CDC) applicable for series RC sensors that requires/prefers sinusoidal excitation is proposed in this paper. The CDC presented works based on a dual-slope technique and it gives a digital output as a function of unknown capacitance of a series RC sensor, i.e., a capacitive sensor with a capacitor and a resistor in series in its electrical equivalent circuit. Output of the CDC is not sensitive to the series resistor. The CDC is useful for grounded as well as floating capacitive sensors, which needs to be excited with a sine wave for best performance. Applications of such capacitive sensors include ice detection, sterility testing of packed food products, etc. A sinusoidal Howland current source can be used to excite a grounded capacitive sensor while a simple current source with a special stabilization scheme that suppresses the effect due to static errors of opamp has been developed for floating capacitive sensor and presented in this paper. A prototype of the proposed CDC for a floating capacitive sensor has been built and tested in the laboratory. Measurement results for the sensor capacitance showed a worst case error of 0.13% for a range of 100 pF, proving the efficacy of the proposed scheme.

Keywords—Capacitance-to-digital converter; capacitive sensor; floating capacitive sensor; current source for capacitive sensors.

I. INTRODUCTION

Accurate, high sensitive, reliable and less expensive sensors are required for various industrial applications such as automation, monitoring of process variables, etc. Same features hold good for requirement of sensors in consumer applications, environmental monitoring, etc. Capacitive sensors possess all these important characteristics and hence widely used in number of scientific and industrial applications. Depending upon the dielectric used, or characteristic of the material under test, the capacitive sensor can be modeled using equivalent circuits in two distinct ways. One is a series RC model shown in Fig. 1(a) which consists of sensor capacitance $C_s$ and a series resistance $R_s$ [1]-[3]. In this model a resistance $R_p$ present in parallel to the sensor is neglected due to its effect being insignificant. The second model shown in Fig. 1(b) is the parallel RC model consisting of the sensor capacitance $C_s$ with a parallel resistance $R_p$. In this case the effect of the series resistance is neglected. This model is a representation for capacitive sensors used in applications such as humidity sensing [4], flow measurement, etc. Most of the available measurement schemes provide capacitance value of the sensor in a parallel model [5]. A CDC suitable for capacitive sensors with parallel RC model is reported in [6]. There are measurement circuits [1], [7] that determine the capacitance value of the sensor in the RC series model. But these techniques do not directly give out a digital value and involve many computational steps for finding out the final value. Thus Capacitance-to-Digital Converter (CDC) that accepts a RC series sensor and provides digital value of the capacitance of the sensor will be very useful. Moreover, in many applications, a sinusoidal excitation is preferred in the measurement of capacitance of the sensors [4], [8], [9]. Thus, it will be advantageous if the CDC employs a sinusoidal excitation for the measurement. Another expected feature of such a CDC is its insensitivity to the variation in the series resistor $R_s$. This paper reports such a CDC that measures and provides digital value of sensor capacitance using sinusoidal excitation.

II. CAPACITANCE-TO-DIGITAL CONVERTER FOR SERIES RC SENSORS

Measurement of the parameters of a sensor represented by the RC series model usually involves passing a known current through the sensor and recording the corresponding output voltage across the sensor. With the advent of silicon technology current sources can be easily realized using opamp circuits. In this paper two types of current sources are considered, based on the type of the sensor employed. The first

![Fig. 1. Equivalent circuit of capacitive sensors. (a) RC series equivalent circuit. (b) RC parallel representation. $C_s$ represents the sensor capacitance while $R_s$ and $R_p$ indicate the resistor in the series and parallel model, respectively.](Image)

![Fig. 2. Howland current source [10] injecting current $v_o/R_1$ into the capacitive sensor, represented by series RC model.](Image)
is a Howland current source [10] (vide Fig. 2) which is used for grounded capacitive loads. A current \( i \) given by \( v_{in}/R_1 \) (when \( R_1 R_x = R_2 R_3 \)) flows through the sensor causing a voltage drop \( v_x \) across it. The output \( v_{o1} (= 2v_x) \) can be given to the proposed converter that will return a digital count corresponding to the value of the sensor capacitance. Measurement circuits based on Howland current source are presented in [11], [12]. Precise matching of resistors is essential for the Howland current source to work efficiently. In case of any mismatch, the current drawn would be influenced by the (load) capacitive sensor [12]. Also the input bias current of the opamp needs to be as low as possible as they tend to saturate the opamp when used for capacitive loads. This is due to the fact that the output impedance offered by the Howland current source is very high in case of dc input [12].

The second current source is for a floating capacitive sensor. A simple circuit that can inject a current \( v_{in}/R_1 \) to the sensor and cause a voltage drop (in voltage \( v_{o1} \)) across it, which vary as a function of change in the capacitance \( C_1 \) is shown in Fig. 3. The voltage \( v_{o1} \) for a \( v_{in} = V_{in}\sin{\omega t} \) is given by

\[
v_{o1} = -\left( R_x / R_1 \right) V_{in}\sin{\omega t} + (1 / \alpha C_x R_1) V_{in}\cos{\omega t}.
\]  

(1)

In (1), \( \omega = 2\pi f_0 \), where \( f_0 \) is the frequency of input excitation. This circuit suffers from static errors of practical opamp. Its output will go to saturation due to bias current of opamp OA1, which passes through the sensor. In order to solve this problem, a modified topology, discussed below is developed.

A. Modified Current Source for Floating Capacitive Sensors

This scheme uses a simple feedback circuit to avoid the effect of static errors such as bias current and offset voltage.

\[
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and a de-integration period of time $T_3$. During the integration period $T_1$, the CLU closes switch $S_1$ and opens switch $S_i$ causing a current $V_o \sin \omega t / R_1$ drawn from the excitation source $V_o = V_n \sin \omega t$ (where $\omega = 2\pi f_n$) to flow through the known capacitance $C_S$. The CLU also keeps switch $S_i$ in position-1 during $T_1$.

The output $v_{o1}$ of opamp $OA_1$ is given as an input to an inverting amplifier of gain -1 (formed by opamp $OA_2$, two equal resistors of value $R_1$) and also to node-1 of switch $S_i$. Further, the inverting amplifier’s output $v_{o3}$ is connected to node-0 of switch $S_i$. The output voltage $v_{o3}$ during $T_1$, denoted by $v_{o1}^T$, changes due to the current flowing through $C_S$ and is expressed in (2). The inverting amplifier’s output $v_{o2}$ (=-$v_{o1}$) during $T_1$, denoted by $v_{o3}^T$, is also given in (2).

$$v_{o1}^T = (V_m / \omega C_S R_1) \cos \omega t \quad \text{and} \quad v_{o3}^T = -(V_m / \omega C_S R_1) \cos \omega t \quad (2)$$

As shown in Fig. 6, a comparator $OC_1$ links the CLU to the $v_{o3}$ with a phase shift of 90°. The CLU looks at the output of comparator $OC_1$ and whenever it is high, sets switch $S_i$ in position-1, otherwise holds it at position-0.

Thus, for the first positive half cycle of input excitation, i.e., from time $t = 0$ to $T_1/2$ (where $T_1 = 1/f_n$), output $v_{o1}$ is high only during $t = 0$ to $T_1/4$, so switch $S_1$ is kept in position-1 for this time connecting output $v_{o1}^T$ to the integrator (formed by opamp $OA_4$, resistor $R_1$ and capacitor $C_i$). A current $I_{I_1} = (V_m / \omega C_S R_1) \cos \omega t$ flows through resistor $R_1$ and also charges the capacitor $C_i$. At $t = T_1/4$, output $v_{o3}$ becomes low, so CLU changes switch $S_i$ to position-0 causing a current $-I_{I_1}$ to charge $C_i$ in the same direction but from signal $v_{o3}^T$. The integrator output $v_{oi}$ changes by $V_{K1}$ (vide Fig. 7) during the first positive half cycle of $v_{oi}$ which can be derived by substituting $v_{o1}^T$ and $v_{o3}^T$ in (3).

$$V_{K1} = \Delta V_{oi}\left[\int_{t=0}^{T_1/2} \frac{V_m}{R_1 C_i} \cos \omega t dt + \int_{T_1/2}^{T_1/4} v_{o3}^T dt \right] \quad (3)$$

$$V_{K1} = -(2V_m / \omega^2 R_1 R_1 C_i C_S) \quad (4)$$

Signal $v_{o1}$ continues to be low till time $t = 3T_1/4$ and the capacitor $C_i$ continues to charge from output $v_{o3}$ as the switch $S_i$ is still in position-0. From $t = 3T_1/4$ to $T_1$, $v_{o1}$ is high, which causes the CLU to move switch $S_i$ to position-1. Now current $I_{I_1}$ charges the capacitor $C_i$ from signal $v_{o1}$.

During the negative half cycle of $v_{oi}$ i.e., from $t = T_1/2$ to $T_2$, output $v_{oi}$ changes by the same amount $V_{K1}$. So, after the completion of one input excitation cycle, the charge accumulated in the capacitor $C_i$ is $2V_m C_i$. This process continues for several excitation cycles till CLU counts time $t = T_1 (= N_1 T_2$, where count $N_1$ represents the number of excitation cycles of $v_{oi}$ during $T_1$). At the end of the integration period the total charge stored in $C_i$ will be

$$Q_i = 2N_1 V_{K1} C_i \quad (5)$$

As soon as integration period ends, the CLU puts switch $S_i$ in position-0 connecting the input of integrator to ground and then closes switch $S_1$ and opens switch $S_2$ (make before break arrangement is provided to avoid amplifier $OA_1$ to operate in open loop mode). The switch $S_2$ is connected to position-0 for a short time $T_o$ so that any switching transients that occur will not be reflected in the integrator output $v_{oi}$. The time $T_o$ is given by $N_o T_2$ where $N_o$ represents number of excitation cycles during which switch $S_2$ is in position-0. After CLU counts time $T_o$, switch $S_i$ is brought back to position-1. Now, current $V_n \sin \omega t / R_1$ flows through the sensor (capacitance $C_i$ with a series resistance $R_1$) causing output voltage of $OA_1$ to change by $v_{o1}^T$, i.e. $v_{o1}$ during $T_2$. This voltage can be represented as in (6), which is also same as (1).
In the de-integration period, the CLU puts switch $S_1$ in position-0 whenever $v_{C1}$ is high and in position-1 otherwise. For $v_{oC} > 0$, the output $v_{C1}$ is high from time $t = T_1$ to $T_1 + T_C/4$, so CLU sets $S_1$ in position-0 giving signal $v_{oi}^{T_2} = -v_{oi}^{T_1}$ to integrator formed by opamp OA1. This causes a current $I_{T_2} = - (R_x / R_x) V_m \sin \omega t + \left( \frac{1}{\omega C_x R_x} \right) \omega t \cos \omega t$ to flow through resistor $R_1$ and charge the capacitor $C_x$. As output $v_{C1}$ becomes low from $t = T_1 + T_C/4$ to $T_1 + T_C/2$, $S_1$ is moved to position-1. A current $-I_{T_2}$ flows through $R_1$ from $v_{oi}^{T_1}$ and charges capacitor $C_x$. The change $V_{K2}$ in output $v_{oC}$ during the positive half cycle of input excitation is given by

$$V_{K2} = \Delta v_{oC}^{T_1 + T_C/2} = \frac{- R_x}{R_1 C_x} \left[ \int_{T_1}^{T_1 + T_C/4} v_{oi}^{T_1} dt + \int_{T_1 + T_C/4}^{T_1 + T_C/2} v_{oi}^{T_1} dt \right].$$

By substituting $v_{oi}^{T_1}$ and $v_{oi}^{T_1}$ in (7), we get $V_{K2}$ as

$$V_{K2} = (2V_m / \omega^2 R_x R_x C_x).$$

The switch $S_1$ continues to be in position-1 as $v_{C1}$ is still low. The same current $-I_{T_2}$ charges $C_x$ till time $t = T_1 + 3T_C/4$ when $v_{C1}$ becomes high and CLU changes switch $S_1$ to position-0. Now a current $I_{T_2}$ from $v_{oi}^{T_1}$ charges $C_x$ till the end of the excitation cycle. During the negative half cycle the output $v_{oC}$ changes by $V_{K2}$. The charge acquired by capacitor $C_x$ for one excitation cycle of $v_{oC}$ during $T_2$ is $2V_{K2} C_x$. The CLU continues to change (as described above) the position of switch $S_1$ till output $v_{oC}$ reaches zero. The CLU notes the time $T_2 = (N_2 / N_1)$, where $N_2$ is number of excitation cycles present in $T_2$) when $v_{oC}$ becomes zero. The CLU recognizes the end of de-integration period from a low to high transition at the output $v_{C2}$ of comparator $OC2$. The total charge $Q_T$ (refer (9)) deposited on the capacitor $C_x$ during $T_2$ is equal to the charge $Q_{T2}$ acquired during $T_1$ giving the relation $\left[ Q_T \right] = \left[ Q_{T2} \right]$. By substituting the values of $V_{K1}$ and $V_{K2}$ in the charge balance equation, we get (10).

$$Q_{T2} = 2N_2 V_{K2} C_x,$$

$$N_2 = \frac{N_1}{C_S},$$

$$C_x = \frac{N_2}{N_1} C_S.$$

Thus the unknown sensor capacitance $C_x$ can be obtained in digital domain directly, by reading the de-integration count $N_2$ and multiplying it with a factor $C_S/N_1$ which is a constant as both $C_S$ and $N_1$ are known fixed values. It can also be observed that (11) is not sensitive to change in the series resistance $R_x$. Fig. 8 shows waveforms at the important points in the CDC when the sensor resistance is set as zero. By comparing Fig. 8 and Fig. 7, we can see that the time taken for de-integration $T_{2C}$ is same with and without the sensor resistance $R_x$.

Prior to conversion phase an auto-zero operation is performed so as to ensure that output $v_{oC}$ is zero before the start of the conversion cycle. In auto-zero phase, CLU switches $S_1$ OFF and $S_2$ ON. It then looks at output $v_{oC}$, if $v_{oC}$ is greater than 0, then $v_{c2} = 1$, and CLU sets $S_1$ in position-1 for $v_{oC}$ high and in position-0 otherwise. For $v_{oC} < 0$, $v_{c2} = 0$, now the CLU sets $S_1$ in position-0 for $v_{oC}$ high and in position-1 otherwise. This operation of the CLU causes output $v_{oC}$ to bring to zero. The end of the auto-zero phase is detected by the CLU from a high to low transition if $v_{oC} > 0$ and a low to high transition if $v_{oC} < 0$. 

![Waveforms at cardinal points in the CDC](image.png)
A prototype of the proposed CDC has been built and tested in the laboratory. Values of the components used in the prototype were $R_1 = 220 \ \Omega$, $C_1 = 1 \ \mu \text{F}$, $R_2 = 27 \ \text{k}\Omega$ and known capacitance $C_s = 100 \ \text{pF}$. Ompamps were realized using the low offset IC OPA227. Switches $S_1$ and $S_2$ were implemented using low ON resistance SPST IC MAX4601. Switches $S_3$ and $S_4$ were realized using SPDT switch IC CD4053. The task of the comparator was accomplished using high speed comparator IC LM311. The 90° phase shift was obtained using an all-pass filter. The function of the CLU was realized using a microcontroller IC MSP430G2553. A frequency 8.192 kHz (derived from a crystal clock of 32,768 kHz) was utilized as the clock to the counter in the CLU. The integration preset count $N_1$ was set at 6144 so that there are integer number of excitation cycles present during integration. The excitation frequency employed was 1 kHz. The low-pass filter for the modified current source was designed with a cut-off frequency of about 0.5 Hz. A dc gain of 15.6 was set using the resistor $R_2$ and fed back to the non-inverting terminal of opamp $OA_1$ ($R_{11} = R_{12} = 330 \ \text{k}\Omega$). In order to emulate the sensor, a standard capacitance box having an accuracy of ±0.1% manufactured by Neptun, Geteisried, Germany was selected and connected in series to a fixed resistance $R_s = 56.250 \ \Omega$. The value of the resistance was measured using a 6-1/2 digit multimeter manufactured by Agilent Technologies. A snapshot of the output $v_{oc}$ along with the output of comparator $OC_2$, for one conversion cycle is shown in Fig. 10. After completion of the integration and the de-integration periods the CLU sets switch $S_1$ in position-0 (connecting input of integrator $OA_1$ to ground) for a predefined time $T_2$ so that any switching transients that occur during $T_2$ in the outputs of $v_{o1}$ and $v_{o3}$ will not affect integrator voltage $v_{oc}$. This short duration between $T_1$ and $T_2$ is visible in Fig. 10. The capacitance $C_s$ was varied from 100 pF to 200 pF in steps of 5 pF and its corresponding digital output count $N_2$ was recorded. Percentage error with respect to the full-scale count was calculated for each change in the sensor capacitance $C_s$ and plotted along with acquired digital output $N_2$ in Fig. 9. Worst case error noted for the measurement of capacitance was found to be 0.13% showing the efficacy of the proposed CDC.

## IV. Conclusion

A new capacitance-to-digital converter that directly reads the digital value of capacitance of a series RC sensor is demonstrated. This CDC is well suited for all types of capacitive sensors and especially for sensors that prefer a sinusoidal excitation for improved performance. A prototype of the CDC has been developed and interfaced with a standard variable capacitor, along with a series resistor and tested in the laboratory. The CDC measured the capacitance accurately and its practicality has been established.

## V. References


