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Impact of lanthanum doped zirconium oxide ($LaZrO_2$) gate dielectric material on FinFET inverter

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Abstract

Fin-typed field effect transistor (FinFET) has considered a suitable device for low power and high-performance applications. The incorporation of gate dielectric lanthanum doped zirconium oxide ($LaZrO_2$) in the 14 nm silicon on insulator (SOI) FinFET not only enhanced effective carrier mobility but also diminished the short channel effects (SCEs). The FinFET embodiment with $LaZrO_2$ has dwindled subthreshold swing (SS), reduced drain-induced barrier lowering (DIBL), and raised on-current to off-current ratio as a contrast to SiO_2-based FinFET. A remarkable enhancement of 1.18×, 11×, and 1.3× for transconductance (g_m), early voltage (V_{EA}), and an intrinsic gain (A_v), respectively, have been investigated. Further, $LaZrO_2$-based n-FinFET and p-FinFET devices have devised with equal dimensions. The improved noise margin of 0.375 V using a single-fin FinFET-based inverter circuit has proven the acceptance of this device in a circuit application.

Keywords

FinFET, Inverter, Dielectric, Subthreshold swing, Drain-induced barrier lowering, Transconductance.

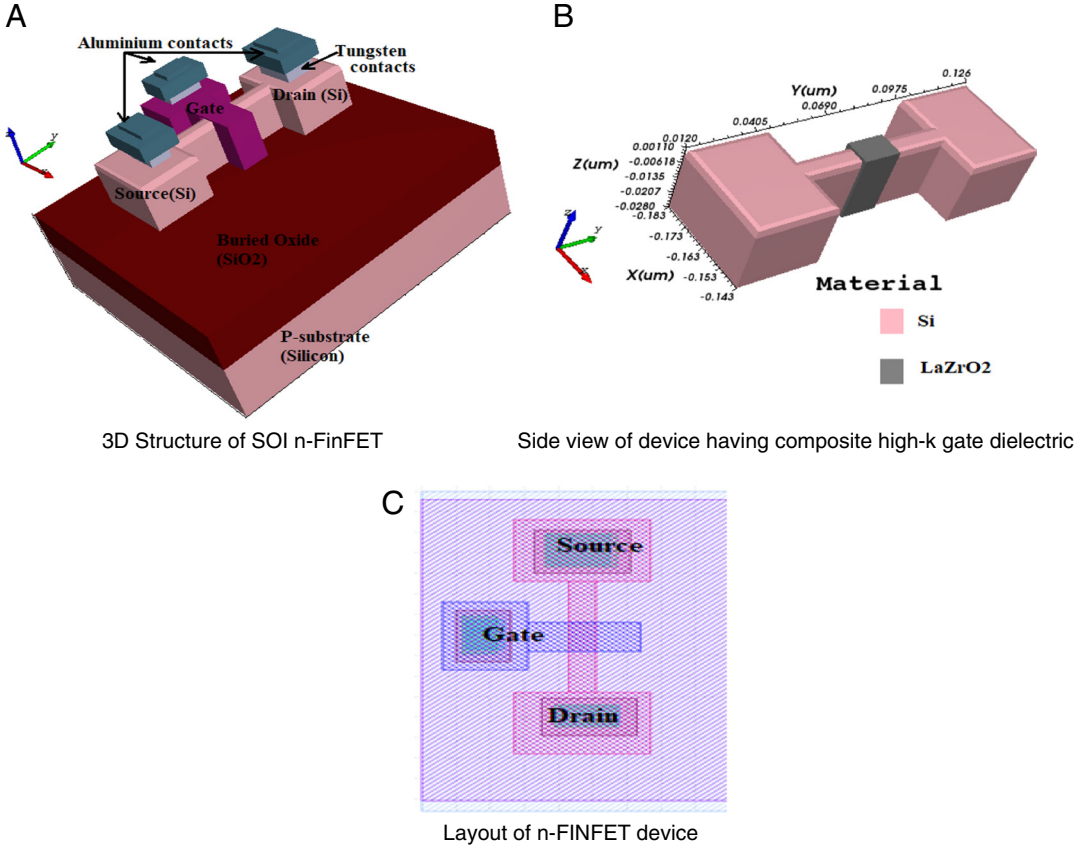
Recently, several miniature devices have developed for low power and high-performance application circuits. It has inspected that fin-typed field effect transistor (FinFET) device shows a substantial reduction in short channel effects (SCEs) as well as leakage current, better switching rate, and consumes less power in comparison to other devices (Gargini, 2020; Colinge, 2008; Sachid and Chenming, 2012). For satisfying the need for the latest portable appliances such as mobile phones, microprocessors, cache memories in computers, the FinFET device has been considered as an appropriate solution. Most of the semiconductors industries such as Samsung, Intel, TSMC, and global foundries are utilizing FinFET devices in their latest processors (Businesswire, 2017). The authors have designed the FinFET-based accumulator to store temporary data bits in the memory (Sathya et al., 2017). FET-based biosensors have also been developed with the help of evolutionary algorithms for biomedical applications. Thus, this device includes additional features viz. high switching speed, low leakage, and small size, making it a prominent substitute in every application field (Sharma and Kumar, 2019a, 2019b; Pindoo and Sinha, 2020; Rathee et al., 2019). Higher leakage current and subthreshold slope in GAA-FET make it unsuitable for low power applications. The device design with novel materials remains the target research area for the IC design engineers. In sub-22 nm technology, the direct tunneling gate leakage current has reduced with novel high-k gate dielectric materials like Al_2O_3 ($k = 9$), ZrO_2 (25), HfO_2 (25), TiO_2 (80), Y_2O_3 (15), Ta_2O_5 (22), $LaZrO_2$ (40), and CeO_2 (23-26). It has observed that for suitable future scaling, a dielectric with k over 40 is preferred, and lanthanum doped zirconium oxide ($LaZrO_2$) has been considered as the promising high-k gate dielectric material for sub-22 nm node FinFET devices (Gaskell et al., 2007; Zhao et al., 2012; Liu et al., 2019; Cheng et al., 1999; Wikipedia 14nm process, 2020).

In this work, the impact on the performance of 14 nm SOI FinFET has been analyzed with conventional SiO_2 and high-k gate dielectric materials, $LaZrO_2$. Further, n-FinFET (N channel FinFET) and p-FinFET (P channel FinFET) devices of the same dimensions have been devised using common gate material (workfunction = 4.6 eV) and LaZrO2 ($k = 40$) as gate oxide material (Zhao et al., 2011). The inverter circuit designed with these devices explained its suitability in circuit applications. The proposed circuit's performance has been analyzed by calculating the noise margin of a single fin configuration. The noise margin (0.375 V) of the simulated inverter circuit has revealed 17% progress as compared to results claimed for the nanowire field-effect transistor (0.32 V) based inverter circuits (Nayak et al., 2014).

The paper has been organized as: the second section explained the design and simulation methodology of the device. Next, the third section discussed the results of the designed FinFET device and its comparison with existing work. Subsequent the fourth section illustrated the performance of FinFET-based inverter. The impact of temperature and voltage variations on the circuit's noise margin has also been described in the same section. In the last section, the conclusion and future scope of work have been discussed.

Device specifications and simulation methodology

The 3D structures of n-FinFET with different perspectives have shown in Figures 1 and 2. Table 1 illustrates the device design considerations for n-FinFET and p-FinFET. The novel material $LaZrO_2$ ($k = 40$) high-k gate dielectric has been used for 14 nm FinFETs (Zhao, Zhao, Werner, Taylor and Chalker, 2012; Cheng et al., 1999; Zhao, Zhao, Tao, Werner, Taylor and Chalker, 2012; Kaur et al., 2019). Table 2 describes the important technology computer-aided design (TCAD) device parameters of 14 nm processes for an inverter model, according to International Technology Roadmap for Semiconductors (ITRS) (Wikipedia 14nm process, 2020; Zhao et al., 2011, 2012; Nayak et al., 2014; Kaur et al., 2019; Genius



3D Structure of SOI n-FinFET

Side view of device having composite high-k gate dielectric

Layout of n-FINFET device

Figure 1: Bird eye view of SOI n-FinFET: (A) 3D structure of SOI n-FinFET, (B) Side view of device having composite high-k gate dielectric, (C) Layout of n-FINFET device.

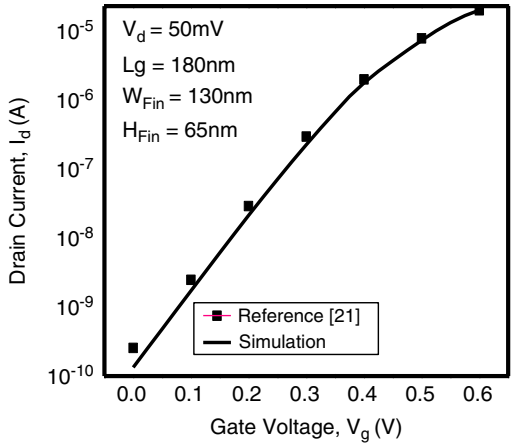


Figure 2: I_d-V_g characteristics of FINFET with reference (de Andrade et al., 2011) and simulation.

User Guide, 2009; Ana and Din, 2011). The simulator's validity has been examined by matching its results with published experimental data in the TCAD environment at 300 K as shown in Fig. 2 (de Andrade et al., 2011). Therefore, it shows that this paper's models and parameters are valid (Genius User Guide, 2009).

Table 1. Structural parameters used in simulation *As per ITRS dimensions (Wikipedia 14nm process, 2020).

Device's performance parameters	Simulation work (n-FinFET)	Simulation work (p-FinFET)
Gate length, L_g (nm)	14	14
Transistor fin pitch (nm)	42	42
Transistor fin width, W_{Fin} (nm)	8	8
Transistor fin height, H_{Fin} (nm)	24	24
Workfunction, WF (eV)	4.6	4.6
Gate dielectric permittivity, k	40	40
Physical oxide thickness (nm)	1.1	1.1
Supply voltage, V_d (volts)	0.75	0.75

Table 2. Important TCAD device parameters for an inverter design.

Process parameters	Value
Design rule unit lambda (μm)	0.007
Thickness of substrate region (μm)	0.03
Height of fin (μm)	0.024
Thickness of gate oxide (μm)	0.0011
S/D doping concentration (donor) for nMOS (cm^{-3})	3E20
S/D doping concentration (acceptor) for pMOS (cm^{-3})	3E20
Supply voltage, V_d (V)	0.8 V
Thickness of buried oxide (μm)	0.02
Thickness of poly-silicon gate (μm)	0.002
Thickness of ILD dielectric (μm)	0.008
Thickness of ILD Metal 1(μm)	0.008
Lateral characteristic length of S/D doping of nMOS (μm)	0.004
Vertical characteristic length of S/D doping of nMOS (μm)	0.003
Doping concentration in p-type substrate (cm^{-3})	1E16
Doping concentration in body (cm^{-3})	1E17

The proposed devices have simulated using the following models:

1. Drift diffusion model (DDM), which solves a particular set of Poisson equations, as mentioned in the following equation:

$$\nabla.\varepsilon\nabla\psi = -q(p - n + N_D^+ - N_A^-) \quad (1)$$

where ψ is the electrostatic potential of the vacuum level; n and p represents the electron and hole concentration; N_D^+ and N_A^- represents the ionized doping concentration; q is an electron charge. The lattice temperature is kept uniform throughout the drift diffusion model.
2. Lombardi surface mobility model has been introduced to address carrier mobility in the inversion layer of the designed device. A cumulative carrier mobility spanning doping-based bulk mobility (μ_B), mobility degradation, scattering due to acoustic phonon (μ_{ac}), and

scattering because of surface roughness (μ_{SR}) is given by:

$$\mu_S^{-1} = \mu_B^{-1} + \mu_{ac}^{-1} + \mu_{SR}^{-1} \quad (2)$$

3. Kane's model can explain the generation of carriers through band to band tunneling (G^{BB}) and expressed as:

$$G^{BB} = A.BBT.\frac{E^2}{\sqrt{E_g}}\exp\left(= B.BBT.\frac{E_G^{\frac{3}{2}}}{E}\right) \quad (3)$$

where E denotes electrical field magnitude; E_G represents the band gap; $A.BBT$ and $B.BBT$ are experimental fitting parameters.

4. The carrier recombination process is elaborated by Shockley–Read–Hall (SRH) model which has defined in the following equation:

$$U_{SRH} = \frac{pn - n_{ie}^2}{\tau_p[n + n_i e^{\frac{E_T}{KT_L}}] + \tau_n[p + n_i e^{\frac{E_T}{KT_L}}]} \quad (4)$$

where τ_n and τ_p are carrier lifetime which are reliant on doping concentration; n_i denotes the intrinsic carrier concentration; E_T is energy trap level; T_L is lattice temperature (Kaur et al., 2019; Genius User Guide, 2019). The variation of electrostatic surface potential along the channel length for $k=40$ has outlined in Figures 3 and 4 illustrates the simulation procedure in visual TCAD for devising FinFET.

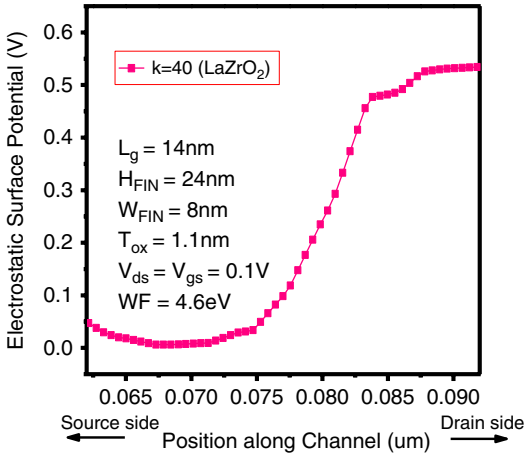


Figure 3: Variation of electrostatic surface potential along the channel length for $k=40$, high-k gate dielectric constant.

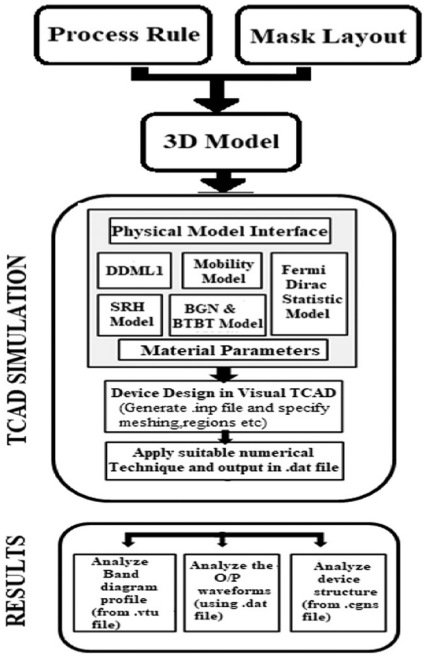


Figure 4: Flowchart of the simulation procedure involved in visual TCAD.

The set of performance parameters evaluated for the designed structure are drain current at highest value of gate voltage (I_{ON}); drain current at lowest value of gate voltage (I_{OFF}); I_{ON}/I_{OFF} current ratio; subthreshold swing ($SS=\partial V_g/\partial \log 10 I_d$); drain-induced barrier lowering (DIBL); threshold voltage (V_t); transconductance ($g_m=\partial I_d/\partial V_g$); transconductance generation factor ($TGF=g_m/I_d$); output transconductance ($g_d=\partial I_d/\partial V_d$); intrinsic gain ($A_V=20\times\log 10(g_m/g_d)$, and early voltage ($V_{EA}=I_d/g_d$). These parameters have been computed with gate voltage (V_g) variation of 0 to 0.75V and drain voltage (V_d) 50mV and 0.75V as the boundary condition. The difference of gate voltage corresponding to both 20mV and 0.75V drain voltage at drain current (I_{DIBL}) of 4×10^{-7}A evaluates DIBL with the formulae stated in the following equation:

$$I_{DIBL} = \frac{W_{eff}}{L_g}\times 10^{-7} A \quad (5)$$

where W_{eff} indicates channel effective width which has measured from the following equation:

$$W_{eff} = 2H_{Fin} + W_{Fin} \quad (6)$$

The constant current method has been used to extract the value of threshold voltage (Siebel et al., 2012).

Results and discussion

The transfer characteristics of n-FinFET in log and a linear scale for L_g=14 nm, V_g=0 to 0.75 V, and V_d=0.75 V has outlined in Figure 5. It has been observed that extracted I_{ON} (4.95×10^{-5}) and I_{OFF} (3.61×10^{-14}) showed thrice enhancement and 10^{-4} factor reduction as compared to the results claimed for the same technology (Lee, 2016; Nirmal et al., 2012). The impact on the performance of the n-FinFET device due to conventional SiO_2 and novel high-k gate dielectric materials, $LaZrO_2$ have been justified in Table 3. The device optimizations of n-FinFET and p-FinFET have done using work function engineering to obtain the improved results for an inverter circuit.

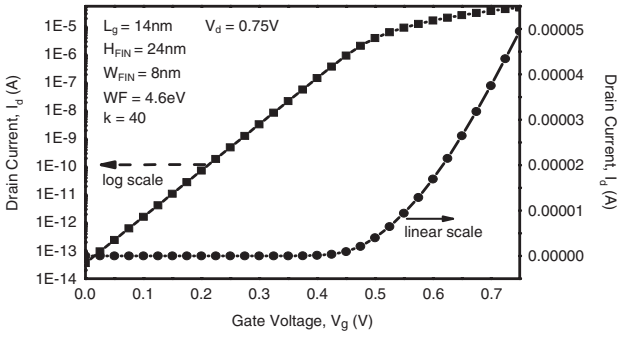


Figure 5: Transfer characteristics of n-FinFET in log and linear scale for L_g = 14 nm, V_g = 0 to 0.75 V and V_d = 0.75 V.

Impact of conventional and novel dielectric oxides on n-FinFET performance

The novel high-k gate dielectric material $LaZrO_2$ has integrated with the n-FinFET device. This material is chemically stable in contact with Silicon and has high crystallization temperature, high dielectric constant and wide energy band gaps (~6 eV) as compared to SiO_2. It has deposited on an active silicon channel by atomic layer deposition (ALD) and chemical vapor deposition (CVD) method at high temperature (Gaskell et al., 2007; Zhao et al., 2012; Liu et al., 2019; Chen et al., 2004). The on-current showed the progress of 2.7× and off-current demonstrated diminishing by 10^{-1} in high-k gate dielectric compared to conventional SiO_2. Due to advancements in carrier transport efficiency, increased electron velocity at the source side, and higher gate capacitance, this further

Table 3. Impacts of gate dielectric SiO_2 and $LaZrO_2$ on the performance of n-FinFET device.

	Simulated n-FinFET	
Parameters (V_d = 0.75 V, V_g = 0.75 V)	**Gate dielectric (LaZrO2) k = 40**	**Gate dielectric (SiO2) k = 3.9**
I_{ON} (A)	4.95×10^{-5}	1.78×10^{-5}
I_{OFF}(A)	3.61×10^{-14}	$5.02E\times10^{-13}$
I_{ON}/I_{OFF}	1.37×10^{9}	3.50×10^{7}
V_t (V)	0.253	0.207
SS(mV/dec)	60.3	67.02
DIBL(mV/V)	10.1	43
g_m (S) (at V_g = 50 mV)	2.42×10^{-4}	2.69×10^{-5}
V_{EA} (V) (at V_g = 50 mV)	10.7	0.88
TGF (V^{-1}) (at V_g = 50 mV)	24.55	23.2266
g_d (S) (at V_g = 50 mV)	1.8×10^{-15}	1.95×10^{-12}
A_V (dB) (at V_g = 50 mV)	183	139.7

improves I_{ON}/I_{OFF} ratio. It depicted that the achieved current rate for $LaZrO_2$ increased by a magnitude of 10^2 orders compared to SiO_2, as outlined in Table 3. This type of device's operation in the subthreshold region can lead to faster switching (Eng et al., 2018; Knoblinger et al., 2008). It has been noticed that the optimum threshold (V_t) for $k=40$ is 26.1 mV in the linear region, which is near to an ideal value. A large V_t in standby mode produces low leakage current. Hence, it has been recognized that a device with high dielectric permittivity value is suitable for realizing VLSI circuits (Pradhan et al., 2014; Mohapatra et al., 2015).

The incorporation of high-k dielectric material increases electrostatic potential near the drain region, increases gate capacitance, and reduces DIBL, as shown in Figure 3. The theoretical value of SS is 60 mV/dec at 300 K and has obtained for the case of high-k gate dielectric material. The percentage reductions of 10 and 76% for SS and DIBL, respectively, have been achieved in comparison to SiO_2. The smaller DIBL results in low leakage current and lower SS leading to better on/off switching performance (Zhao et al., 2011; Kaur et al., 2018, 2020a, 2020b; Aujla and Kaur, 2019; Eng et al., 2018). The enhanced I_{ON} leads to better g_m, as it decides the transistor's gain and operating speed. The g_d dwindled by order of magnitude 10^{-3} and g_m embellished by a factor of 1.18× compared to conventional material. The low value of g_d and g_m's high value is desirable for analog circuits, and small g_d increases V_{EA} and A_V (Nayak et al., 2014; Kaur et al., 2019; Pradhan et al., 2014; Mohapatra et al., 2015). In MOSFET, V_{EA} is the hypothesized intercept of saturation output characteristics on the V_d axis. A remarkable augmentation for V_{EA} and A_V has been noticed.

Comparison of n-FinFET performance with existing work

The performance parameters for the n-FinFET device, I_{OFF}, and I_{ON}/I_{OFF} decreased by 1,000 times and increased by 100 times, respectively, at the cost of on-current compared to results claimed in the existing literature (Lee, 2016; Karbalaei et al., 2020). The short channel performance parameters viz. SS and DIBL of simulated n-FinFET declined by 22 and 85% compared to previous alleged work (Lee, 2016). The impressive enhancement by a factor of 10× and 4× is pointed out for V_{EA} and A_V compared to 20 nm gate length technology for n-FinFET device (Mohapatra et al., 2015). Therefore, it has verified that the simulated device has improved results for electrical and analog performance parameters compared to the existing literature (Mohapatra et al., 2015).

Performance optimization of n-FinFET and p-FinFET devices using work function engineering

The design optimization of n-FinFET and p-FinFET devices have been done with superior lanthanum doped zirconium oxide gate material. The perfect V-curve for n-FinFET and p-FinFET have established for saturation (at 0.75 V) and linear (at 50 mV) operation as congregated in Figures 6 and 7. The similar performances for both devices are realized due to work function engineering using a mid-gap band of 4.6 eV and are outlined in Table 4 (Eng et al., 2018; Knoblinger et al., 2008). It has been reported that enhancement in value of work function and high-k gate dielectric material improves the current ratio and lessens device's SS (Kaur et al., 2020a, b). Figure 7 signifies the output characteristic curve for both devices at the supply voltage of 0.5, 0.6, 0.75, 0.8, and 0.85 V.

Optimized FinFET-based inverter

An inverter circuit has devised in shorted gate (SG) mode configuration by utilizing optimized n-FinFET and p-FinFET devices. The circuit dimensions have shown in Table 2.

The SG mode configuration has preferred due to the advantage of improved drive strength and

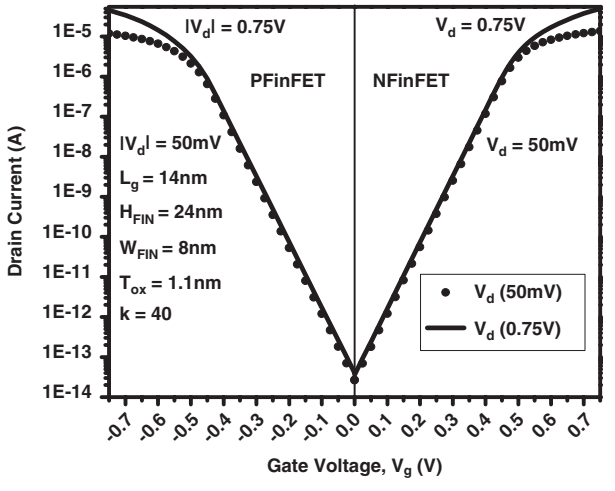


Figure 6: Simulated transfer characteristic of n-FinFET and p-FinFET devices.

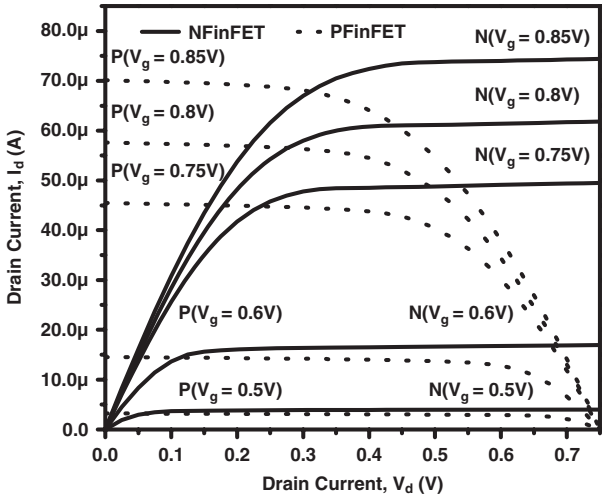


Figure 7: Output characteristics of n-FinFET and p-FinFET devices for same dimensions: $L_g = 14$ nm, $H_{FIN} = 24$ nm, $W_{FIN} = 8$ nm, $T_{ox} = 1.1$ nm, WF (N) = 4.6 eV, and $k = 40$.

gate-controlled channel. The schematic layout of the designed FinFET-based inverter and structural dimensions has presented in Figure 8. Further, noise margins (NM) have been measured for analyzing the performance of the circuit.

It has defined as the maximum allowable spurious signal accepted by a device without affecting the circuit (VLSI System Design, VLSI Basics, 2019; Yeh et al., 2018). The butterfly curve (VTC) of the FinFET-based inverter has delineated in Figure 9 for

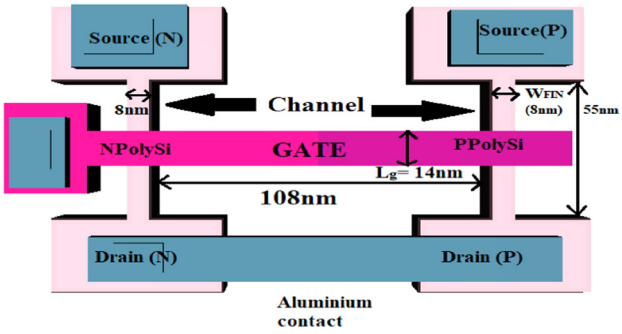


Figure 8: Schematic layout of optimized FinFET-based inverter circuit with dimensions ($H_{Fin} = 24$ nm, $T_{ox} = 1.1$ nm, $k = 40$ and WF = 4.6 eV).

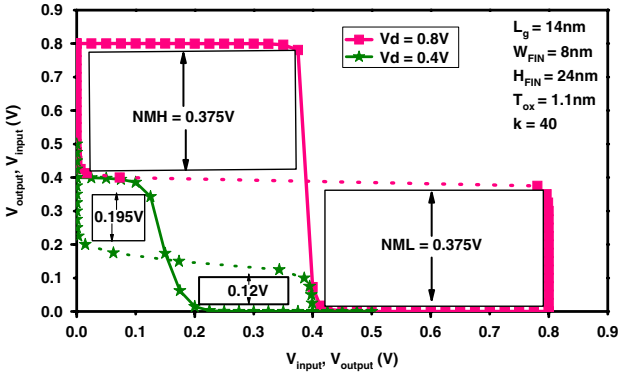


Figure 9: Butterfly curve for proposed FinFET-based inverter (n-FinFET and p-FinFET of equal size) at 0.8 and 0.4 V supply voltage.

Table 4. Performance analysis of FinFET devices.

	n-FinFET		p-FinFET	
Metrics	**Lin ($V_d = 50$ mV)**	**Sat ($V_d = 0.75$ V)**	**Lin ($V_d = 50$ mV)**	**Sat ($V_d = 0.75$ V)**
I_{ON} (A)	1.37×10^{-5}	4.95×10^{-5}	1.81×10^{-5}	4.54×10^{-5}
I_{OFF}(A)	2.64×10^{-14}	3.61×10^{-14}	2.69×10^{-14}	3.98×10^{-14}
I_{ON}/I_{OFF}	0.51×10^{9}	1.37×10^{9}	0.67×10^{9}	1.14×10^{9}
SS (mV/dec)	59.9	60.3	59.9	60.9
V_t (V)	0.261	0.253	0.262	0.253
g_m (S)	5.88×10^{-5}	2.42×10^{-4}	4.71×10^{-5}	2.33×10^{-4}
TGF (V^{-1})	24.68	24.55	24.65	24.37
DIBL (mV/V)	10.1	12.3		

two different voltages. It inferred that the devised inverter circuit performs satisfactory at a low supply voltage of 0.4 V. The estimated high noise margin (NMH) and low noise margins (NML) at a supply voltage of 0.8 and 0.4 V are 0.375, 0.375 V and 0.195, 0.12 V, respectively. The NM of the simulated circuit is improved by 17% (0.375 V) as compared to results derived by authors for nanowire field-effect transistor-based inverter (0.32 V) (Nayak et al., 2014). The determined static power consumption for a circuit is 3×10^{-14}W (Li et al., 2007).

The dependence of noise margin on temperature (273, 300, 398 K) and voltage (0.4, 0.8, 1.2 V) variations have been analyzed for $LaZrO_2$ gate dielectric and delineated in Table 5. It perceived that the increased operating voltage and reduced temperature induces improvement in the noise margin. The degraded noise margin has been observed for lower voltage and higher temperatures (Chakraborty et al., 2013; Bortolon, 2018; Pattanaik et al., 2012).

Conclusion and future scope

The impact of compound high-k gate dielectric $LaZrO_2$ on the device's performance has studied using Cogenda TCAD with the drift-diffusion transport framework. The incorporation of high-k dielectric in SOI FinFET devices improves its scalability, reduces chip area, and enhances the storage capacity, making it suitable for high-speed applications and memories. It has been found that the proposed device demonstrates superior SCEs immunity by giving a 10% reduction in SS and 76% decrement in DIBL for $LaZrO_2$ gate oxide compared to SiO_2 gate oxide. The I_{ON}/I_{OFF} has improved by two orders of magnitude compared to results claimed in previous generations of MOSFET devices (Lee, 2016). The significant improvements for analog parameters viz. g_m (5.88×10^{-5} S), V_{EA} (10.7 V), and A_V (183 dB) in the linear region have also been observed, which evaluate its suitability in circuit applications. Further, optimized n-FinFET and p-FinFET devices have been devised for implementing an inverter. A remarkable advancement in NM (0.375 V) of an inverter circuit has been realized compared to acceptable NMs mentioned in the research paper (Nayak et al., 2014). Although the proposed device and its inverter circuit present progress, therefore SRAM implementation can be done in the future.

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Table 5. Impact on noise margin due to temperature and voltage variation for simulated inverter circuit

Gate dielectric permittivity value(k)	Temperature (kelvin)						Voltage (volts)					
	273 K		300 K		398 K		0.4 V		0.8 V		1.2 V	
	NMH (V)	NML (V)	NMH (V)	NML (V)	NMH (V)	NML (V)	NMH (V)	NML (V)	NMH (V)	NML (V)	NMH (V)	NML (V)
40($LaZrO_2$)	0.4	0.377	0.375	0.375	0.35	0.35	0.195	0.12	0.375	0.375	0.55	0.55

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